



PTO/SB/08a (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1

of

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Complete if Known

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|------------------------|--------------------|
| Application Number | 09/961,202 |
| Filing Date | September 24, 2001 |
| First Named Inventor | Baruch SOLOMON |
| Art Unit | 2186 |
| Examiner Name | Zhuo H. Li |
| Attorney Docket Number | 02207/12173 |

U.S. PATENT DOCUMENTS

| Examiner Initials * | Cite No. ¹ | Document Number | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|------------------------|--------------------------|--|--------------------------------|--|---|
| | | Number - Kind Code ² (if known) | | | |
| Z | | US-6,535,959 | 03-18-03 | Ramprasad et al. | |
| | | US-6,507,921 | 01-14-03 | Buser et al. | |
| | | US-6,427,188 | 07-30-02 | Lyon et al. | |
| | | US-6,351,844 | 02-2002 | Bala | |
| | | US-6,339,822 | 01-15-02 | Miller | |
| | | US-6,279,103 | 08-21-01 | Warren | |
| | | US-6,233,678 | 05-15-01 | Bala | |
| | | US-6,216,200 | 04-10-01 | Yeager | |
| | | US-6,189,140 | 02-13-01 | Madduri | |
| | | US-6,185,675 | 02-06-01 | Kranich et al. | |
| | | US-6,076,144 | 06-2000 | Peled et al. | |
| | | US-6,073,213 | 06-2000 | Peled et al. | |
| | | US-5,974,538 | 10-26-99 | Wilmot, II | |
| | | US-5,966,541 | 10-12-99 | Agarwal | |
| | | US-5,924,092 | 07-1999 | Johnson | |
| | | US-5,913,223 | 06-15-99 | Sheppard et al | |
| | | US-5,889,999 | 03-30-99 | Breternitz, Jr., et al. | |
| | | US-5,461,699 | 10-24-95 | Arbabi et al. | |
| | | US-4,575,814 | 03-11-86 | Brooks, Jr., et al. | |
| | | | | | |

FOREIGN PATENT DOCUMENTS

| Examiner Initials * | Cite No. ¹ | Foreign Patent Document | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | English Abstract |
|------------------------|--------------------------|---|--------------------------------|---|---|---------------------|
| | | Country Code ³ - Number ⁴ - Kind Code ⁵ (if known) | | | | |
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**INFORMATION DISCLOSURE
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Sheet 2

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| Application Number | 09/961,202 |
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| First Named Inventor | Baruch SOLOMON |
| Art Unit | 2186 |
| Examiner Name | Zhuo H. Li |
| Attorney Docket Number | 02207/12173 |

NON PATENT LITERATURE DOCUMENTS

| Examiner Initials * | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
|------------------------|--------------------------|---|----------------|
| zh | | Conte et al, "Optimization of Instruction Fetch Mechanisms for High Issue Rates," <i>Proceedings of the 22nd Annual Int'l. Symposium on Computer Architecture</i> , June 22-24, 1995, Santa Margherita Ligure, Italy, pp. 333-344. | |
| | | Dutta et al, "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors," <i>Proceedings of the 28th Int'l. Symposium on Microarchitecture</i> , Nov. 29-Dec. 1, 1995, Ann Arbor, MI, pp. 258-263. | |
| | | Hennessy et al., <i>Computer Organization and Design: the hardware/software interface</i> , 2 nd Edition, Morgan Kaufmann Publishers, San Francisco, CA, 1998, p. 570. | |
| | | Johnson, Mike, <i>Superscalar Microprocessor Design</i> , PTR Prentice-Hall, Englewood Cliffs, New Jersey, 1991, Chapter 10, pages 177-202. | |
| | | Jourdan et al, "eXtended Block Cache," Intel Corporation, Intel Israel, Haifa, 31015, Israel, pages 1-10. | |
| | | McFarling, Scott, "Combining Branch Predictors," June 1993, WRL Technical Note TN-36, Digital Western Research Laboratory, Palo Alto, CA, 25 pp. | |
| | | Michaud et al, "Exploring Instruction-Fetch Bandwidth Requirement in Wide-Issue Superscalar Processors," <i>Proceedings of the 1999 Int'l. Conference on Parallel Architectures and Compilation Techniques</i> , Oct. 12-16, 1999, Newport Beach, CA, pp. 2-10. | |
| | | Patel et al, "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing," <i>Proceedings of the 25th Annual Int'l. Symposium on Computer Architecture</i> , June 27-July 1, 1998, Barcelona, Spain, pp. 262-271. | |
| | | Reinman et al, "A Scalable Front-End Architecture for Fast Instruction Delivery," <i>Proceedings of the 26th Int'l. Symposium on Computer Architecture</i> , May 2-4, 1999, Atlanta, GA, pp. 234-245. | |
| | | Rotenberg et al, "Trace Processors," <i>Proceedings of 30th Annual IEEE/ACM International Symposium on Microarchitecture</i> , December 1, 1997, Research Triangle Park, NC, pp. 138-148. | |
| | | Solomon et al., "Micro-Operation Cache: A Power Aware Frontend for Variable Instruction Length ISA," <i>ISLPED '01</i> , August 6-7, 2001, Huntington Beach, CA, pp. 4-9. | |
| | | Seznec et al, "Multiple-Block Ahead Branch Predictors," <i>Proceedings of the 7th Int'l. Conference on Architectural Support for Programming Languages and Operating Systems</i> , Oct. 1-4, 1996, Cambridge, MA, pp. 116-127. | |
| ✓ | | Yeh et al, "Increasing the Instruction Fetch Rate via Multiple Branch Prediction and a Branch Address Cache," <i>Proceedings of the 7th Int'l. Conference on Supercomputing</i> , July 1993, Tokyo, Japan, pp. 67-76. | |

Examiner
Signature

Zhuo Li

Date
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12/6/04

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| Application Number | Not assigned |
| Filing Date | September 24, 2001 |
| First Named Inventor | SOLOMON et al |
| Group Art Unit | Not assigned |
| Examiner Name | Not assigned |
| Attorney Docket Number | 2207/12173 |

Sheet 1 of 1

U.S. PATENT DOCUMENTS

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|---------------------|------------|-----------------------|------------------------|---|--|---|
| | | Number | Kind Code 2 (if known) | | | |
| ✓ | | Serial No. 09/736,889 | | Jourdan et al | Filed 12-14-00 | |
| ✓ | | 5,381,533 | | Peleg et al | Jan. 10, 1995 | |

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

| Examiner Initials * | Cite No. 1 | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T 2 |
|---------------------|------------|---|-----|
| ✓ | | Bellas et al, "Architectural and Compiler Techniques for Energy Reduction in High Performance Microprocessors", <i>IEEE Transactions on VLSI Systems</i> , Vol. 8, No. 3, June 2000 | |
| | | Black et al, "The Block-Based Trace Cache", Proceedings of the 26th Intl. Symposium on Computer Architecture, IEEE Computer Society TCCA, ACM SIGARCH, Atlanta, Georgia, May 2-4, 1999 | |
| | | Friendly et al, "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", 30th Annual IEEE/ACM Intl. Symposium on Microarchitecture, Research Triangle Park, North Carolina, December 1-3, 1997 | |
| | | Intrater et al, "Performance Evaluation of a Decoded Instruction Cache for Variable Instruction-Length Computers", 19th Annual Intl. Symposium on Computer Architecture, Gold Coast, Australia, May 19-21, 1992 | |
| | | Jacobson et al, "Path-Based Next Trace Prediction", 30th Annual IEEE/ACM Intl. Symposium on Microarchitecture, Research Triangle Park, North Carolina, December 1-3, 1997 | |
| | | Manne et al, "Pipeline Gating: Speculation Control for Energy Reduction", Proceedings, 25th Annual Intl. Symposium on Computer Architecture, IEEE Computer Society Tech. Comm. on Computer Architecture, ACM SIGARCH, Barcelona, Spain, June 27-July 1, 1998 | |
| | | Glaskowsky, Peter N., "Pentium 4 (Partially) Previewed", <i>Microprocessor Report</i> , Vol. 14, Archive 8, pp. 1, 11-13, August 2000 | |
| | | Papworth, David B., "Tuning the Pentium Pro Microarchitecture", <i>IEEE Micro</i> , IEEE Computer Society, Vol. 16, No. 2, April 1996 | |
| | | Upton, Michael, "The Intel Pentium® 4 Processor", http://www.intel.com/pentium4 , October 2000 | |
| | | Rotenberg et al, "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching", Proceedings, 29th Annual IEEE/ACM Intl. Symposium on Microarchitecture, MICRO-29, IEEE Computer Society Tech. Comm. on Microprogramming and Microarchitecture, Assn. for Computing Machinery SIGMICRO, Paris, France, December 2-4, 1996 | |
| ✓ | | Jourdan et al, "eXtended Block Cache, Proceedings 6th Intl. Symposium on High-Performance Computer Architecture HPCA-6, Toulouse, France, Jan. 8-12, 2000 | |

Examiner Signature

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Date Considered

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